Dr. Philip Endecott

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Date of Birth: 17th May 1970

Summary of Skills and Interests

My skills cover a wide range of subjects from VHDL to databases, allowing me to contribute to interdisciplinary projects involving hardware / software co-design and embedded systems.

Digital Design

- Design of all kinds of digital systems
- Low-power design
- Asynchronous logic
- VHDL simulation and synthesis
- FPGA and ASIC design

Microprocessors

- Implementation of embedded RISC processors
- Quantitative analysis of architectural issues
- Low-power instruction set features

Design Tools

- Implementation of design tools
- HDL simulation
- Processor simulation
- In-circuit debug
- FPGA place&route algorithms

Software

- C, C++
- Unix, Linux in embedded systems
- XML / XSLT
- Web applications
- SQL, Postgres databases

Employment and Education - Summary

March 2004 - present
Self-employed / consultant (see below)

August 2003 - March 2004
Senior Electronics Design Engineer
Adder Technology Ltd.
- Video compression FPGA for a hardware VNC encoder.

August 1999 - April 2002
Member of Technical Staff
AT&T Laboratories Cambridge Ltd.
- Design of a low-power embedded RISC processor and its toolset.

October 1998 - April 1999
Principal Software Engineer
Systolix Ltd. *- Place & route and simulation tools for a DSP FPGA.*

October 1995 - October 1998
Research Associate
“Design Tools for High Speed Asynchronous Circuits”
AMULET Group, University of Manchester.
- Simulation tools for a hardware description language.

October 1993 - October 1995	Ph.D. Student "SCALP: A Superscalar Asynchronous Low-Power Processor" AMULET Group, University of Manchester.
October 1992 - October 1993	M.Sc. Student "Processor Architectures for Power Efficiency and Asynchronous Implementation" AMULET Group, University of Manchester.
September 1991 - July 1992	Support Engineer ARM Ltd. *- ARM's 18th employee!*
September 1988 - June 1991	B.Sc. Student Computer Science (1st Class Hons.), University of Manchester.

Employment and Education - Details

I am currently self employed and divide my time between consultancy work, primarily offering advice about digital FPGA and ASIC design to companies in the Cambridge area that I know personally, and an online venture called **TREEFIC**. This is a web site for family history enthusiasts that uses algorithms similar to those used in PCB and ASIC layout to draw family tree diagrams; it started as a personal project – I was curious to learn more about database and web technology - and now generates a small income.

My last permanent employment was with **ADDER TECHNOLOGY** where I designed and implemented the video compression accelerator for their **AdderLink IP** product. This unit allows remote administration of a computer by connecting to its video, keyboard and mouse ports on one side and Ethernet on the other. A low-cost Xilinx FPGA is used to pre-process the high-speed video data, reducing the load on the main processor and so offering better performance than competing solutions. The main design challenges were the high speeds required for video (up to 165 million pixels/second), interfacing to SDRAM, and minimising cost. The FPGA worked first time.

During my two and a half years at **AT&T LABORATORIES CAMBRIDGE** I was chief architect and hardware designer for the **JCN CPU PROJECT**. JCN was a conventional 32-bit RISC microprocessor, prototyped in an FPGA but also suitable for ASIC implementation. The aim was to give us more flexibility at less cost than we would get buying in a processor IP block for use in lab projects. We also used it as the basis for experiments in low-power design, and through a number of small changes to the instruction set, hardware and tools reduced the activity on the external buses by more than 40%. Several patents are pending on these power-saving inventions.

The JCN project involved two engineers at AT&T and a lecturer on sabbatical from Cambridge University Computer Laboratory. A substantial part of the project was the development of the simulator and in-circuit debugging system. My responsibilities included JTAG in-circuit debugging, the graphical user interface, and configuration of the tool based on the instruction set specification.

The processor core was nearly all written in high-level VHDL and was remarkably small in terms of lines-of-code. The exception was the control circuit providing clock gating and halt/wake-up; I used an asynchronous state-machine synthesis tool to implement this, allowing the processor's clock to be removed in halt mode.

AT&T Laboratories Cambridge closed in April 2002 due to AT&T budget cuts. I spent my redundancy payment on a year-long round-the-world trip.

My previous job was for a start-up company called **SYSTOLIX** who had invented a DSP processor consisting of an array of multiply-accumulate units with FPGA-style interconnect. My role, as the fifth employee, was to implement the required software tools, including FPGA-like place and route, HDL-based simulation and filter synthesis.

Prior to this I spent six years with the **AMULET** group at the University of Manchester, led by professor Steve Furber. The AMULET group is best known for its asynchronous implementations of ARM processors. My postgraduate work looked at how - or rather if - less conventional architectures would be more suited to asynchronous low-power implementation than the ARM. This involved analysis of the power efficiency and code density issues in conventional instruction sets and building a model of a superscalar asynchronous processor.

I then spent three years with the same group as a postdoctoral research associate, developing a hardware description language for high-level modelling of asynchronous systems. The lack of tools had been cited as a reason for the slow adoption of asynchronous techniques in industry. My language, LARD, adds occam-style channel communication to the usual hardware description mechanisms. Use of this language led to a ten-fold improvement in productivity during the initial design phase.

Before starting my Ph.D. I spent a year working for **ARM**, who at that time were a small bunch of hard-working engineers in a barn out in the Cambridgeshire countryside. This gave me a useful insight into start-up companies, chip design, and the chip business. My work included test engineering and code reviewing for a video controller chip, and contributions to what became the AMBA on-chip bus.

Other Skills and Interests

I speak French and Spanish more than adequately for my holidays, having taken GCSE Spanish evening classes some years ago and AS French this year.

I am the author of a small number of open-source software projects, including **Decimail**, a mail server based on a PostgreSQL database, and **Anyterm**, a terminal emulator on a web page.

I enjoy escaping to the hills and have been known to take the Fort William sleeper after work on a Friday when the forecast is for good weather - sun or snow - in the highlands. I am also an occasional caver.